ABSTRACT OF THE DISCLOSURE

Disclosed is a clock regeneration circuit comprising a PLL circuit which includes a voltage control oscillator, for synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of a reception signal; a clock extraction circuit which includes a band passing filter having a passing band width which concurrently extracts a basic waves component of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception signal; a frequency detector for detecting a different in frequencies between an output of the clock extraction circuit and an oscillation frequency of the voltage control oscillator; a filter for controlling the oscillation frequency of the voltage control oscillator of the PLL circuit at a detection output of the frequency detector; a bit rate detection circuit for detecting a bit rate of the reception signal; and a frequency selection circuit for outputting an oscillation frequency of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to the bit rate detected by the bit rate detection circuit, as a regeneration clock signal.